

REMARKS

Claims 1-39 are currently pending in the subject application, and are presently under consideration. Claims 1-39 are rejected. Claims 13, 18, 21, 32, and 35 have been amended. Claims 14 and 34 has been cancelled. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Amendments to the Specification

The Specification has been objected to on the basis of informality. Specifically, the Office Action dated August 11, 2005 (at page 2), requests that the word "risking" on page 7, line 24 be replaced by the word "rising." Appropriate correction has been made in the Amendments to the Specification section above. An additional change at page 11 has been made to correct another typographical error. Withdrawal of the objection to the Specification is respectfully requested.

II. Objection to the Claims

Claims 14 and 32 have been objected to on the basis of informalities. Specifically, the Office Action dated August 11, 2005 (at page 2), requests that the phrase "the timing constraint" in claim 14 be replaced with "a timing constraint." Claim 14 has been cancelled, rendering the objection to claim 14 moot.

The Office Action dated August 11, 2005 (at page 2), also requests that the phrase "a first path" in claim 32 be replaced with the phrase "the first path." Appropriate correction has been made in the amendment to claim 32. In addition, the Office Action dated August 11, 2005 (at page 2), also requests clarification of the phrase "the second path including...at least a portion of the second path;" and "a second downstream path." Claim 32 has been further amended to replace "a second downstream path" with "the at least a second path." Withdrawal of the objection to claim 32 is respectfully requested.

III. Rejection of Claims 1-39 Under 35 U.S.C. §102(b)

Claims 1-39 stand rejected under 35 U.S.C. §102(b) as being unpatentable by U.S. Patent No. 5,740,347 to Avidan ("Avidan"). Claims 13, 18, 32, and 35 have been amended. Claims 14 and 34 has been cancelled. Withdrawal of this rejection as applied to the remaining pending claims is respectfully requested for at least the following reasons.

Claim 1 recites a calculator that provides an indication of slack for at least one node, the indication of slack being determined based on a minimum slack value for paths (being plural form) that include the at least one node, regardless of path transparency. The Office Action dated August 11, 2005, asserts that claim 1 is anticipated by the gray and black box model taught by Avidan (Office Action dated August 11, 2005, page 3, citing numerous sections of Avidan). Representative for Applicant respectfully disagrees with this assertion. Avidan teaches a method for analyzing timing in circuits wherein a gray box model is generated by searching paths from a primary clock input of a circuit to determine best and worst paths amongst the elements of the circuit (Abstract). Avidan also teaches that the system performs timing checks to determine and report timing failures on defined paths, including comparisons between the minimum and maximum timing of the longest path for a setup time and the shortest path for a hold time (see, e.g., col. 11, line 52 through col. 12, line 12). However, nothing in Avidan teaches that any such determination of a minimum slack value for paths that include the node. In claim 1, the minimum slack is being determined for paths (being in plural form) that include the node.

Avidan teaches a mode of operation in which the system reports slack for each path leading to a destination node (col. 10, ll. 30-33 and 52-64). However, Avidan does not teach that a calculator provides an indication of slack for a node, the indication of slack being determined based on minimum slack value for paths that include the node, regardless of path transparency, as recited in claim 1. The discussion of slack in the teachings of Avidan is limited to slack for shortest and longest paths and to reporting timing errors in slack tables (see, e.g., col. 13, ll. 39-48; col. 19, ll. 32-45; col. 20, ll. 21-23). Avidan does not teach that the slack values of multiple paths that include at least one node are employed to determine slack for such node(s) *based on a minimum slack value* for the paths that include such node(s). The discussion of comparisons between minimum and maximum timing of defined paths is limited solely to timing checks for a determination of timing failures. For example, this deficiency in Avidan is further supported by a discussion on calculation of clock skew at col. 11, ll. 20-34, and a discussion regarding setup and hold checks for arrival times of source nodes versus reference nodes, provided at col. 11, line 47 to col. 12, line 12.

Avidan also discloses a gray box model used to verify multiple paths in a circuit design (col. 3, ll. 12-19). The gray box model is taught in Avidan to be a solution for generating timing models of a circuit when latch transparency exists (col. 2, ll. 61-67). Specifically, the approach taught by Avidan reports errors relative to the turn-off edge of the

target clock for transparent latches (col. 12, lines 47-50). Additionally, Avidan teaches that the gray box model is simply used to perform timing checks on paths of the circuit, and not for providing an indication of slack for a node based on a minimum slack value for multiple paths that include the one node, regardless of path transparency, as recited in claim 1.

Avidan teaches that the gray box model reports positive slack in its timing analysis if a signal arrives too early, and reports a setup error if the signal arrives after the latch turns off (col. 19, ll. 32-41). However, the gray box model taught by Avidan disregards path transparency only with respect to timing checks, but fails to teach providing an indication of slack for a node based on a minimum slack value for paths that include the one node, regardless of path transparency, as recited in claim 1.

For the reasons stated above, because Avidan fails to teach each and every element of claim 1, Avidan does not anticipate claim 1. Withdrawal of the rejection of claim 1, as well as claims 2-12 which depend therefrom, is respectfully requested.

Claim 4 further recites a plurality of latches that are clocked by substantially out of phase clock signals. In contrast, the only discussion regarding the clocking of latches in Avidan describes that “two latches are expected to be in the same phase and the second latch will be expected to be transparent.” Col. 12, ll 41-46. Since Avidan fails to teach the subject matter recited in claim 4, claim 4 and its dependent claims (claims 5 and 6) are not anticipated by Avidan.

Claim 9, which depends from indirectly from claims 1, 7, and 8 , recites a potential slack calculator that ascertains a minimum slack value associated with the at least one node according to a minimum of the slack determined for the paths traced by the path tracer. The Office Action dated August 11, 2005, asserts that claim 9 is taught by Avidan (at page 5, citing Avidan, col. 11, line 35 through col. 12, line 40). Representative for Applicant respectfully disagrees. As discussed above, Avidan does not teach that a minimum slack value is determined for (plural) paths associated with a node. The cited section describes minimum and maximum timing checks for source nodes and reference nodes. Avidan fails to teach that a minimum slack value is determined for such traced paths associated with a node, and, consequently, Avidan does not teach a potential slack calculator that ascertains a minimum slack value associated with the at least one node according to a minimum of the slack determined for the paths traced by the path tracer, as recited in claim 9. Accordingly, withdrawal of the rejection of claim 9 is respectfully requested.

Amended claim 13 recites a path tracer that traces paths associated with a given node of a circuit design, regardless of path transparency, the path tracer tracing at least one path that includes an input path to the given node and at least another path that includes a downstream portion relative to the given node, and a calculator that determines slack characteristics associated with the traced paths associated with the given node based on timing information for the traced paths. The calculator selects a minimum slack characteristic from the slack characteristics determined for the traced paths associated with the given node. Similar to the reasons discussed above with respect to claim 1, Avidan does teach or suggest that slack for a given node might be determined based on slack determined for plural paths that include the given node. That is, the approach disclosed in Avidan is fundamentally different from the system recited in claim 13. Withdrawal of the rejection of claim 13, as well as claims 15-20 which depend therefrom, is respectfully requested.

Claim 18 has been amended consistent with the amendments to claim 13. Amended claim 18 recites a potential slack calculator that determines a potential slack as the minimum slack characteristic that is associated with the given node based on the slack characteristics determined for each of the traced paths. Since Avidan fails to determine such a potential slack, as discussed above regarding claims 1 and 9, Avidan does not anticipate claim 18. Withdrawal of the rejection of claim 18 is respectfully requested.

Claim 21 has been amended to recite means for determining potential slack for a given node, the potential slack corresponding to a minimum slack value determined from slack values for each of a plurality of paths that include the given node based on timing information for the plurality of paths. Since Avidan fails to teach any means for determining a minimum slack value, as recited in amended claim 21, and for substantially the same reasons as stated above regarding claims 1 and 9, Avidan does not anticipate amended claim 21. Withdrawal of the rejection of claim 21, as well as claims 22-26 which depend therefrom, is respectfully requested.

Claim 27 recites a computer readable medium having computer-executable instructions for performing a method that includes computing slack associated with a given node by analyzing each path associated with the node transparently. In contrast, as discussed above with respect to claim 1, Avidan does not compute slack for a given node by analyzing other paths transparently. Instead, Avidan computes slack for a node by examining only such node. Consequently, since the analysis function recited in claim 27 is absent from the teachings of Avidan, the determination of potential slack value as a minimum of the

computed slack is also absent from the teachings of Avidan.. For these reasons as well as for those stated above regarding claims 1 and 9, Avidan does not anticipate claim 27.

Withdrawal of the rejection of claim 27, as well as claims 28-31 which depend therefrom, is respectfully requested.

Claim 32 has been amended to recite that method includes determining a slack characteristic for first and second paths associated with a node of a given circuit design, and providing an indication of slack associated with the node according to a minimum of the slack characteristic for the first path and the slack characteristic for the second path. For the reasons stated above regarding claim 1, Avidan does not anticipate amended claim 32. Withdrawal of the rejection of claim 32, as well as claims 33 and 35-39 which depend therefrom, is respectfully requested.

For the reasons described above, claims 1-13, 15-33 and 35-39 are patentable over the cited art. Accordingly, withdrawal of this rejection is respectfully requested.

IV. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

By:

Gary J. Pitzer
Registration No. 39,334
Attorney for Applicant(s)

CUSTOMER NO.: 022879

Hewlett-Packard Company
Legal Department MS 79
3404 E. Harmony Road
Ft. Collins, CO 80528